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AMENDMENT TO THE CLAIMS:

LISTING OF CLAIMS:

5 This listing of claims replaces all prior versions, and listings, of claims in the
referenced application.

Claims 1-5 cancelled.

1 Claim 6. (Currently amended, Allowable)) A tri-stable CMOS latch, having
2 first and second inputs for receiving first and second input signals, respectively, where the
3 first and second input signals have first and second signal levels, and with combinations of
4 the signal levels of the first and second input signals defining first, second, and third ternary
5 logic states, said tri-stable CMOS latch ternary logic signals in either a first, second, or third
6 state, comprising:
7 a first series circuit coupling first and second supply voltage terminals, with
8 the first series circuit including a first PMOS transistor, including source, drain, and gate
9 terminals coupling the first supply voltage terminal to a first node, a first biasing element
10 coupling the first node to a second node, and a first NMOS transistor, including source, drain,
11 and gate terminals coupling the second node to the second supply voltage terminal;
12 a second series circuit coupling the first and second supply voltage terminals,
13 with the second series circuit including a second PMOS transistor, including source, drain,
14 and gate terminals coupling the first supply voltage terminal to a third node, a second biasing
15 element coupling the third node to a fourth node, and a second NMOS transistor, including
16 source, drain, and gate terminals coupling the fourth node to the second supply voltage
17 terminal;
18 a feedback network coupling the first node to the gate terminal of the second
19 NMOS transistor, the second node to the gate terminal of the second PMOS transistor, the
20 third node to the gate terminal of the first NMOS transistor, and the fourth node to the gate
21 terminal of the first PMOS transistor;
22 with said first and second biasing elements, and said MOS transistors
23 fabricated utilizing MOSFET technology, where said first and second biasing elements are
24 diode-connected transistors, and with the first and second biasing elements creating unequal

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25 voltage drops to bias the PMOS and NMOS transistors in one of the first and second series
26 circuits in a higher-current state and the PMOS and NMOS transistor of the other of the first
27 and second series circuits in a lower-current state to achieve first and second stable operating
28 points when the first and second input signals having signal levels defining a ternary signal in
29 the first or second ternary logic states are is received and creating substantially identical
30 voltage drops to bias the PMOS and NMOS transistors in both the first and second series
31 circuits in triode mode to achieve a third stable operating point, where the first and second
32 PMOS and NMOS transistors conduct substantially the same current; when the first and
33 second input signals having signal levels defining a ternary logic signal in the third ternary
34 logic state are is received.

1 Claim 7. (Thrice amended, Allowable) A MOS circuit comprising:
2 a current source;
3 a first clocking transistor having source, drain, and gate terminal with said
4 source terminal coupled to the current source, where the first clocking transistor conducts
5 when a first control signal, received at said gate terminal, is asserted;
6 a tristable MOS latch including:
7 first and second inputs for receiving first and second input signals,
8 respectively, where the first and second input signals have first and second signal
9 levels, and with combinations of the signal levels of the first and second input signals
10 defining first, second, and third ternary logic states ~~ternary logic signals in either a~~
11 ~~first, second, or third state;~~
12 a first series circuit coupling a first supply voltage terminal to the drain
13 terminal of said first clocking transistor, with the first series circuit including a first
14 load element coupling the first supply voltage terminal to a first node, a first biasing
15 element coupling the first node to a second node, and a first MOS transistor, including
16 source, drain, and gate terminals coupling the second node to the drain terminal of
17 said first clocking transistor;
18 a second series circuit coupling a first supply voltage terminal to the
19 drain terminal of said first clocking transistor, with the second series circuit including
20 a second load element coupling the first supply voltage terminal to a third node, a
21 second biasing element coupling the third node to a fourth node, and a second MOS

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22 transistor, including source, drain, and gate terminals coupling the fourth node to the
23 drain terminal of said first clocking transistor;
24 a feedback network coupling the first node to the gate terminal of the
25 second MOS transistor and third node to the gate terminal of the first MOS transistor;
26 with said first and second load elements, said biasing elements, and
27 said MOS transistors fabricated utilizing MOSFET technology and with the first and
28 second load and biasing elements creating unequal voltage drops to bias one of the
29 MOS transistors in a higher-current state and the other MOS transistor in a lower-
30 current state to achieve first and second stable operating points when the first and
31 second input signals having signal levels defining a ternary signal in the first or
32 second ternary logic states are is received and creating substantially identical voltage
33 drops to bias the MOS transistors in triode mode to achieve a third stable operating
34 point, where the first and second MOS transistors conduct substantially the same
35 current; when the first and second input signals having signal levels defining a ternary
36 logic signal in the third ternary logic state are is received;
37 a second clocking transistor having source, drain, and gate terminal with its
38 source terminal coupled to the current source, where the second clocking transistor conducts
39 when a second control signal, received at said gate terminal, is asserted;
40 an input circuit including:
41 first and second circuits respectively coupling the first and third nodes
42 to the drain terminal of the second clocking transistor, with the first circuit including a
43 first input transistor having source, drain, and gate terminals, the first input transistor
44 coupled to the first input to receive a first input signal at said gate terminal and with
45 the second circuit including a second input transistor having source, drain, and gate
46 terminals, the second input transistor coupled to the second input to receive a second
47 input signal at said gate terminal;
48 where the tristable latch holds any of the first, second, or third ternary logic
49 states applied to the first and second inputs when the first control signal is asserted and the
50 second control signal is not asserted.

1 Claim 8 and 9. (Cancelled)